

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLAS
DRAFTSMAN		

FIG 1

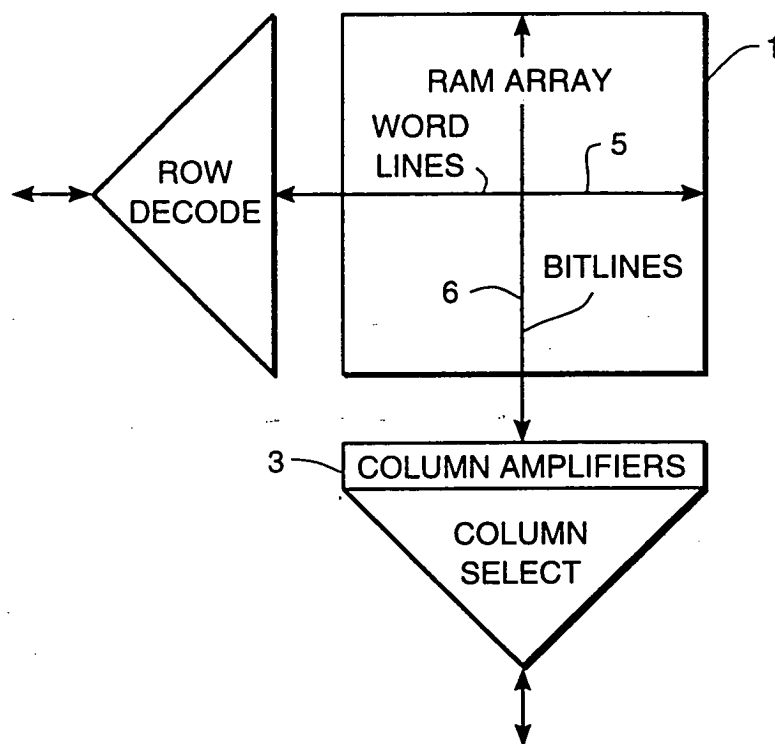
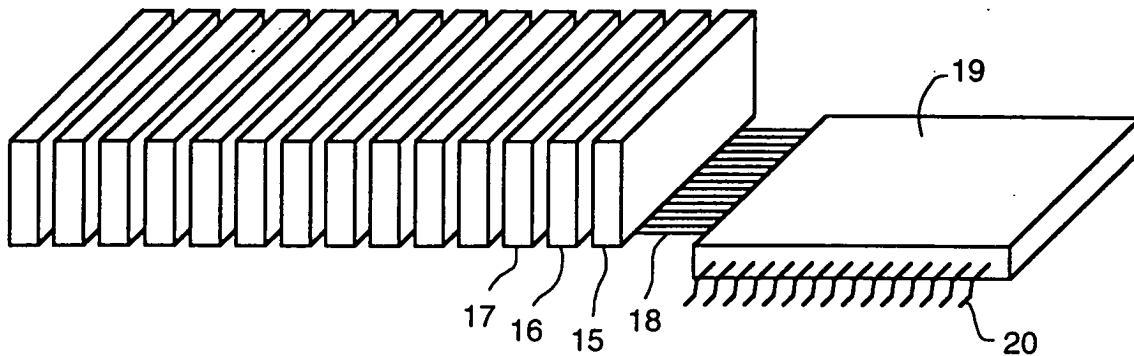


FIG 3



REGULAR ACCESS

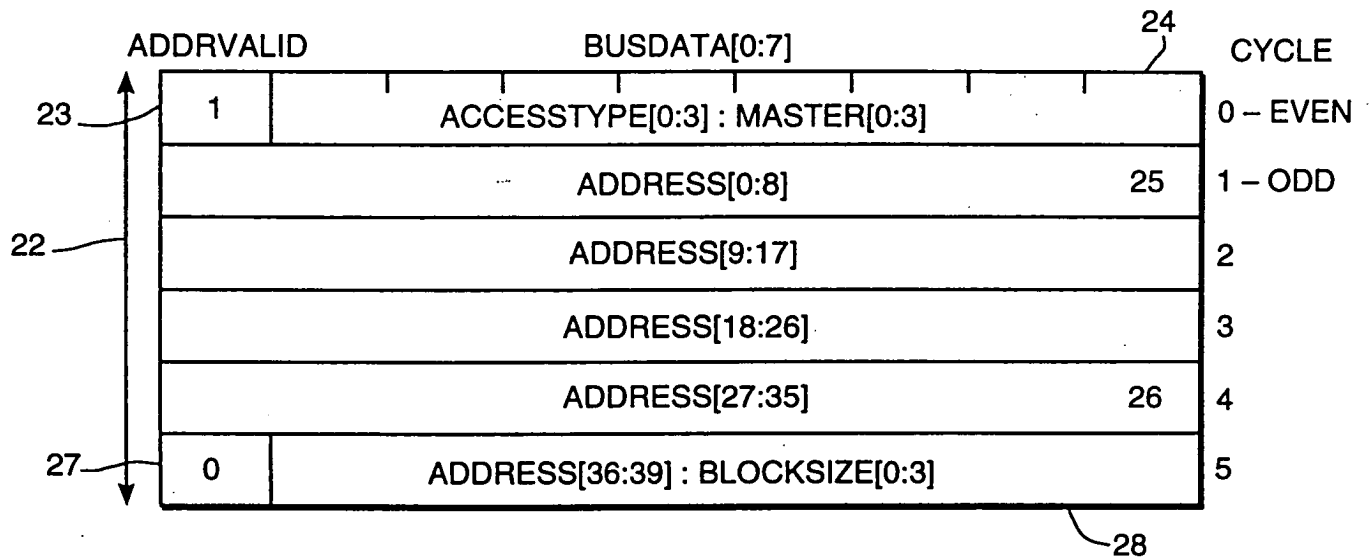


FIG 4

REJECT (NACK) CONTROL PACKET

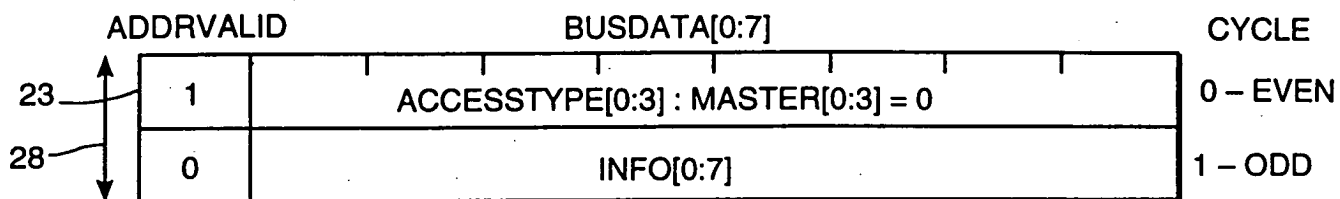


FIG 5

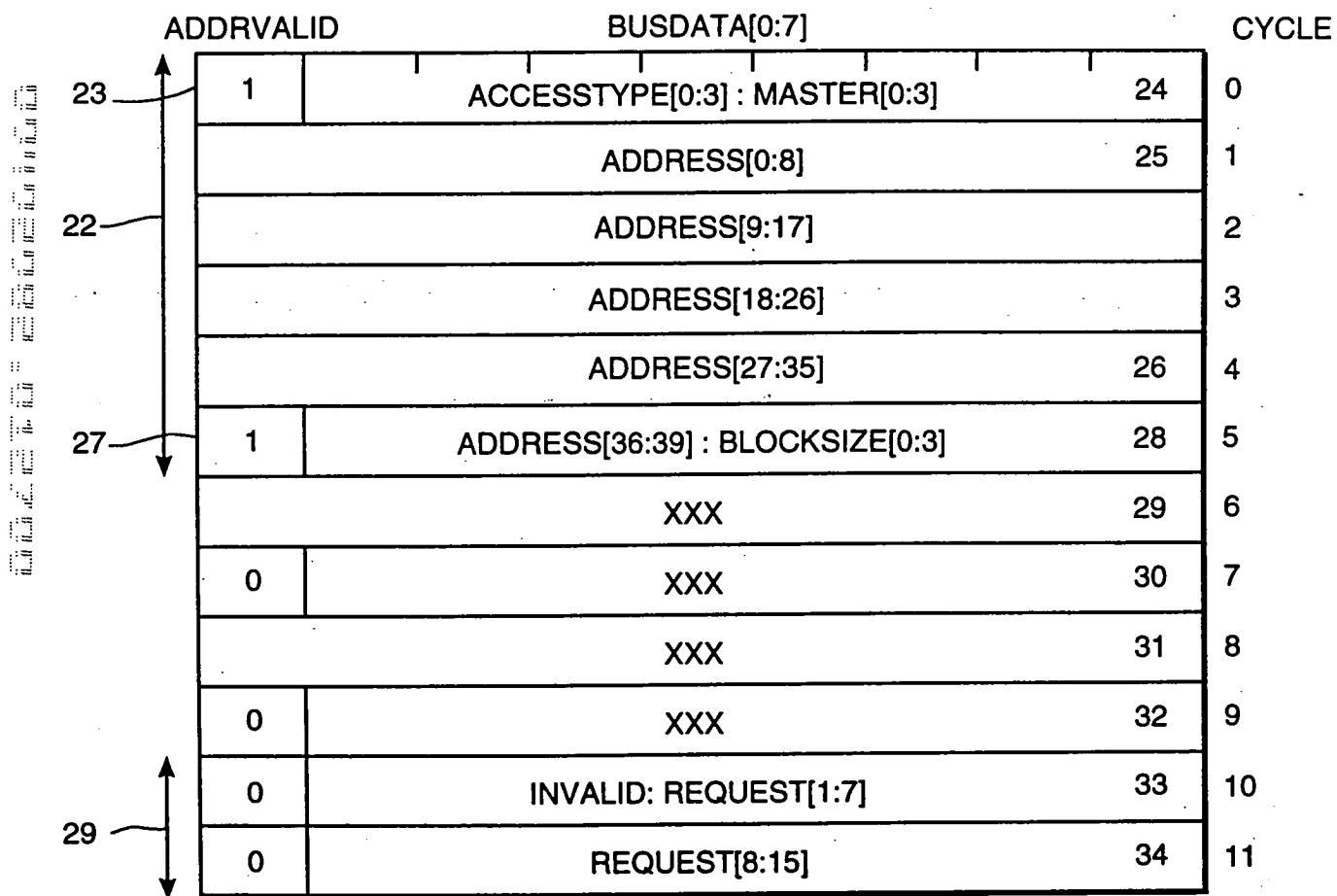


FIG 6

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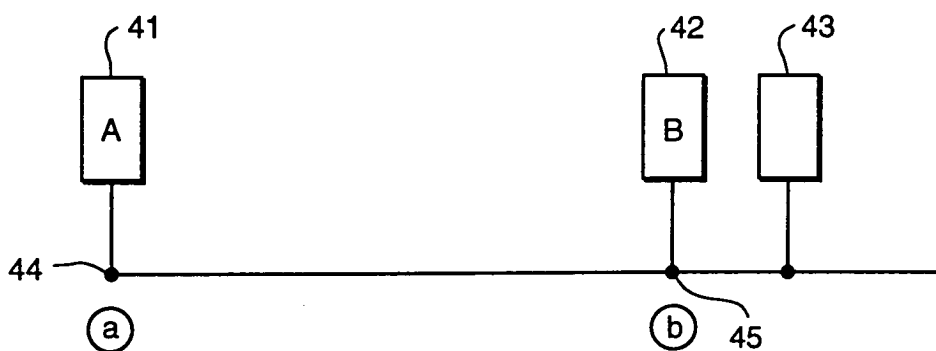


FIG 7A

VOLTAGE LOGICAL
VALUE

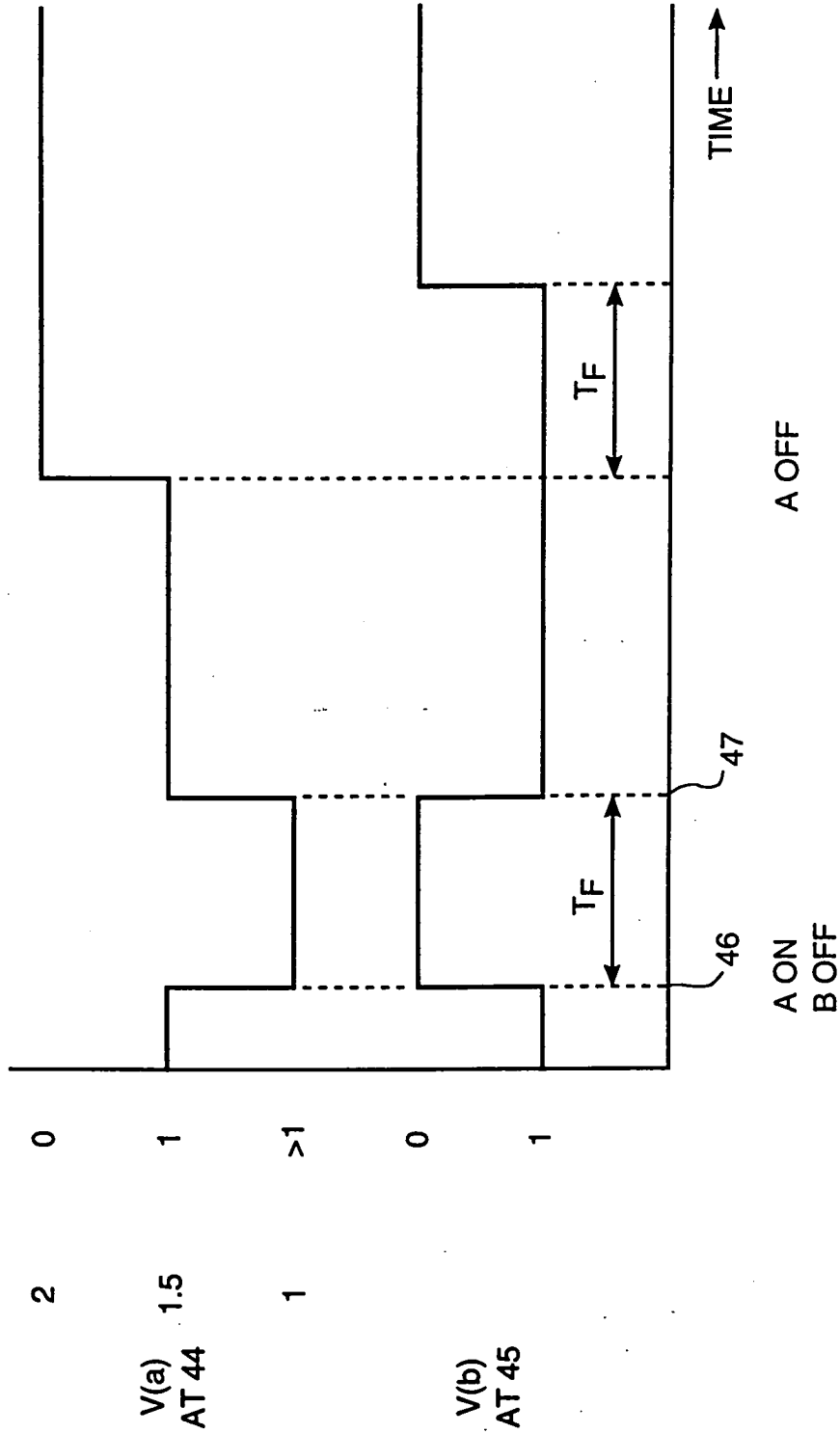


FIG 7B

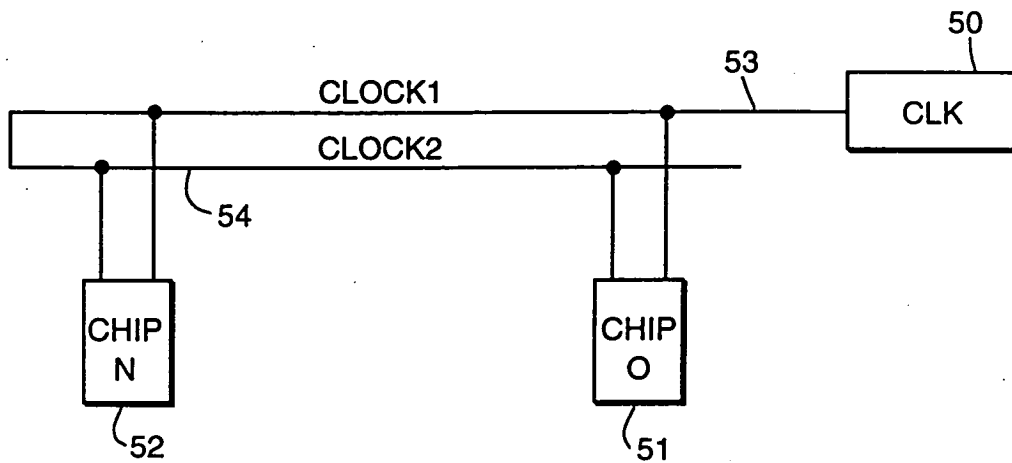


FIG 8A

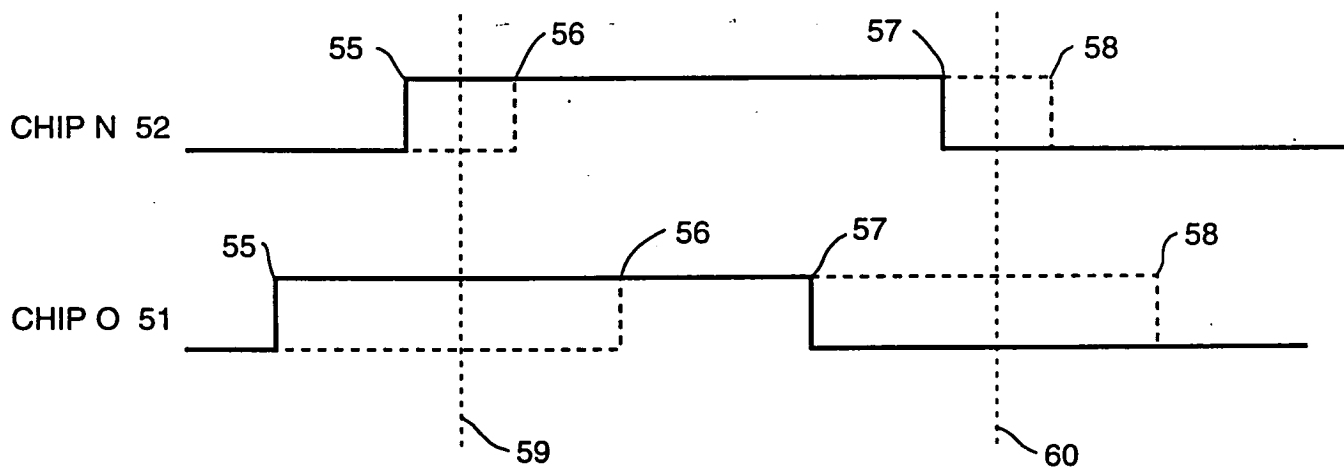
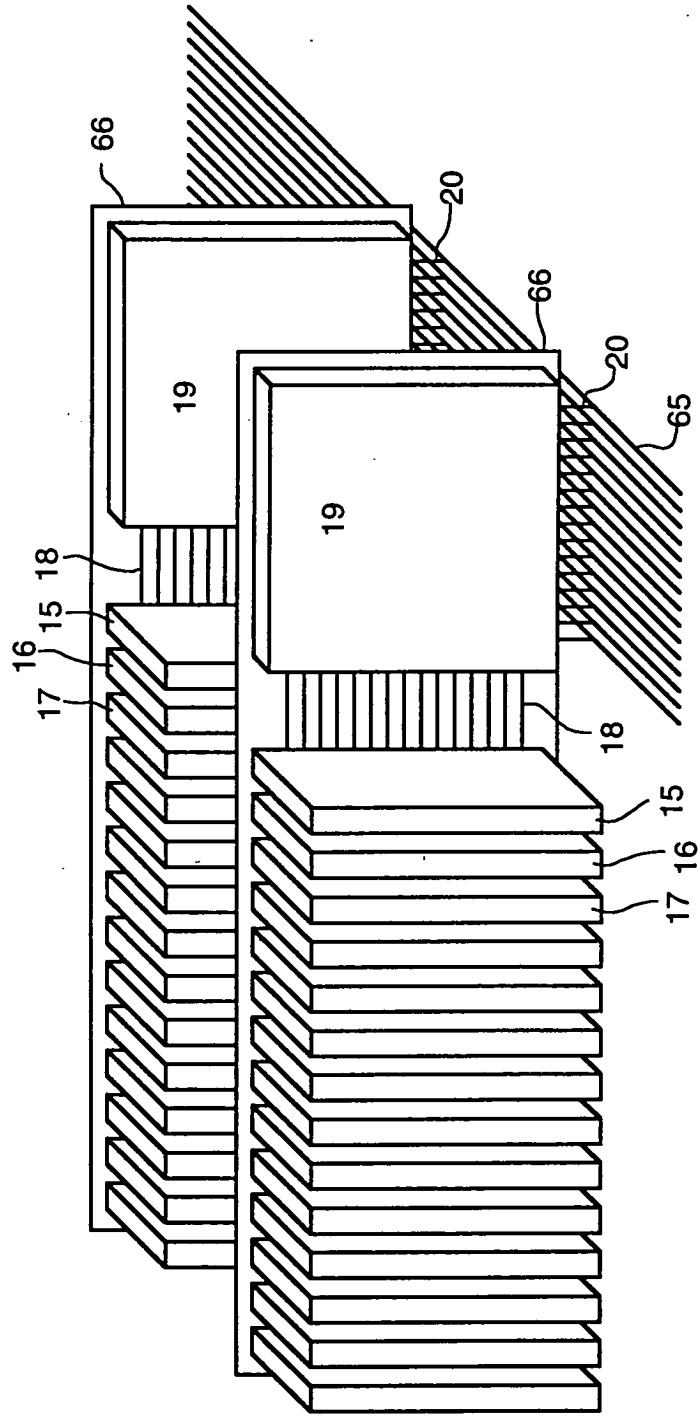


FIG 8B

FIG. 9



Block diagram of a differential signal processing circuit. The circuit includes an input signal line (68) that splits into two paths. The first path passes through a buffer (76) and a multiplexer (75) to output lines. The second path passes through two input registers (71, 72) and a multiplexer (73) to output lines. The registers are clocked by CLK and CLK-bar signals. A reference signal (68) is also provided.

THE

FIG 11

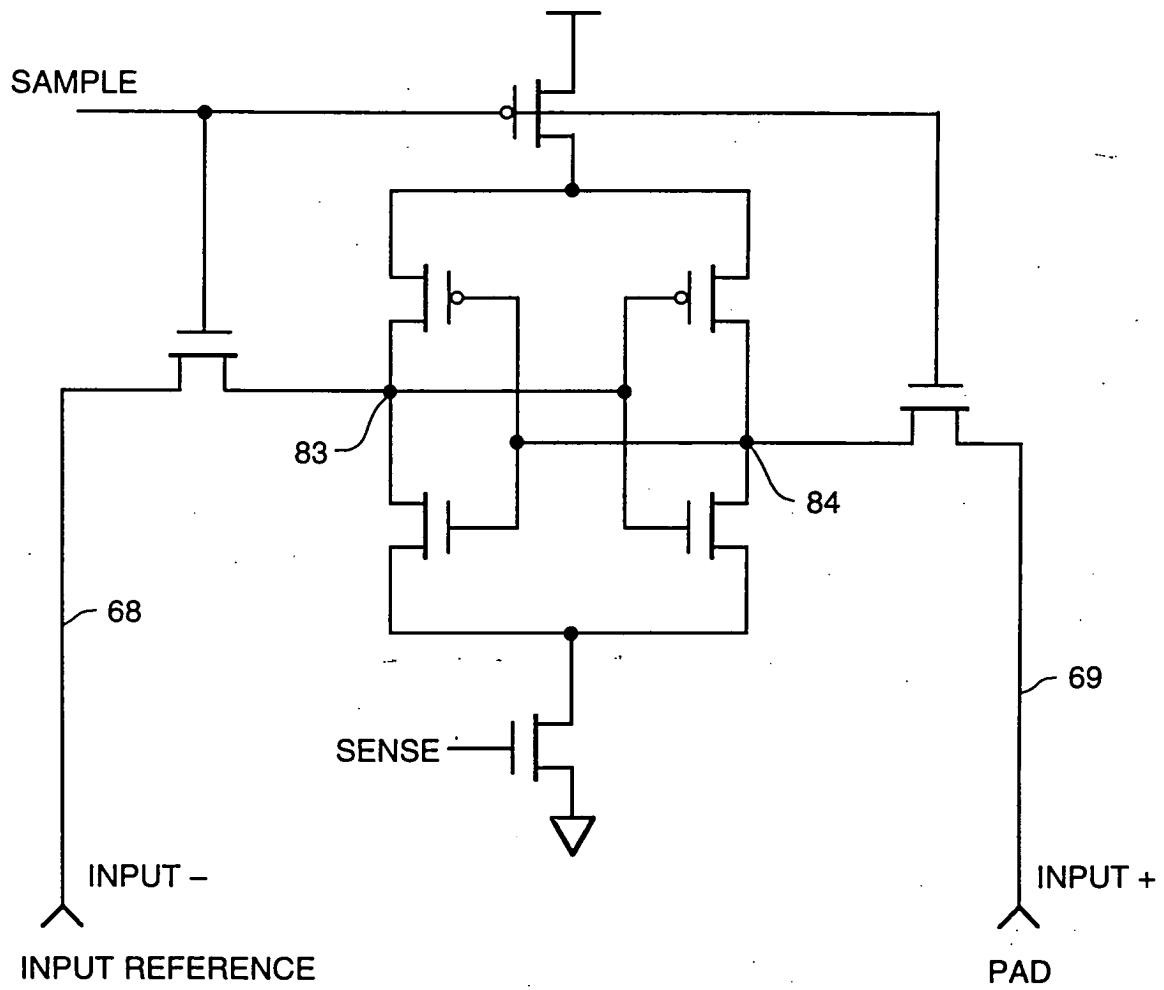


FIG 12

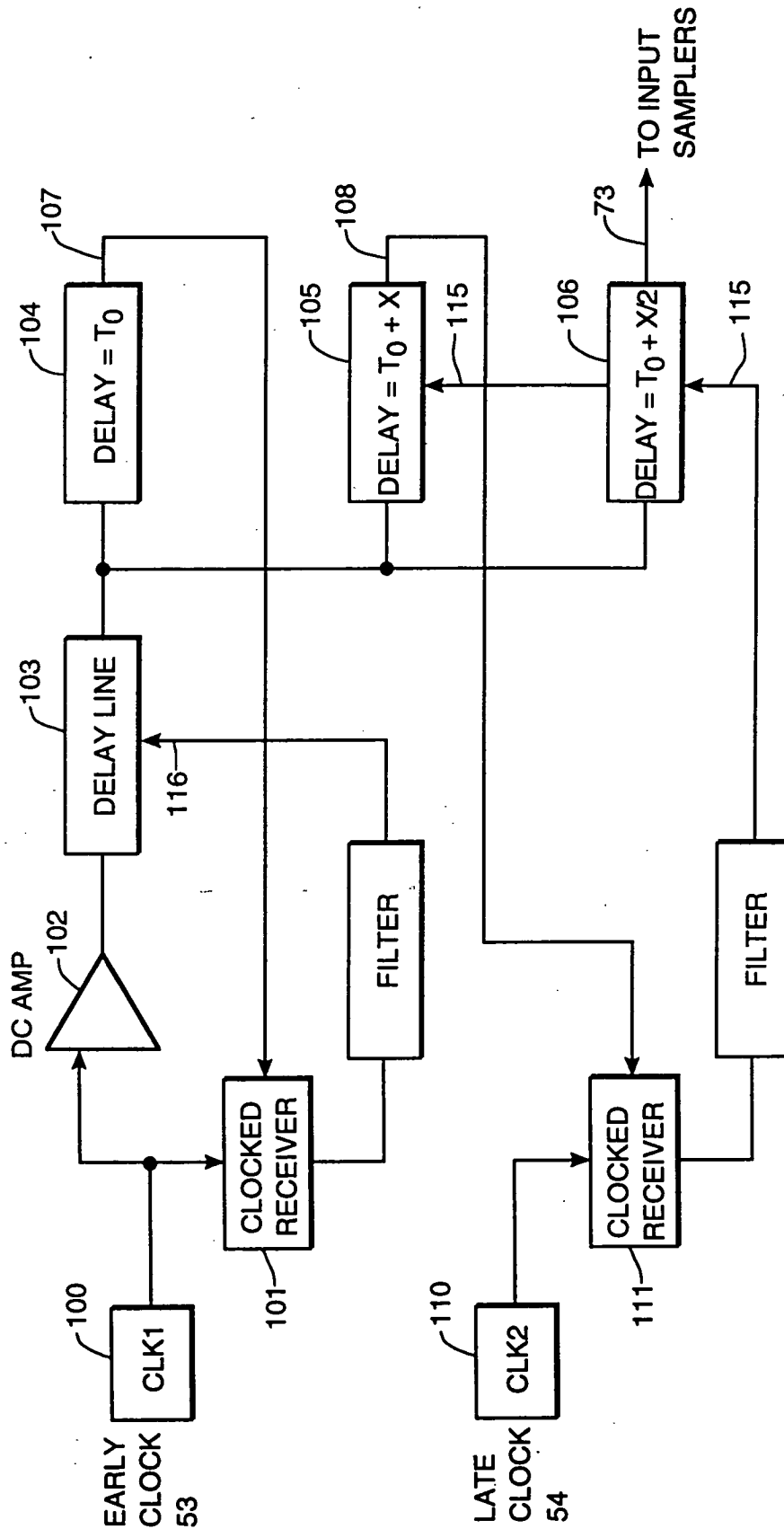
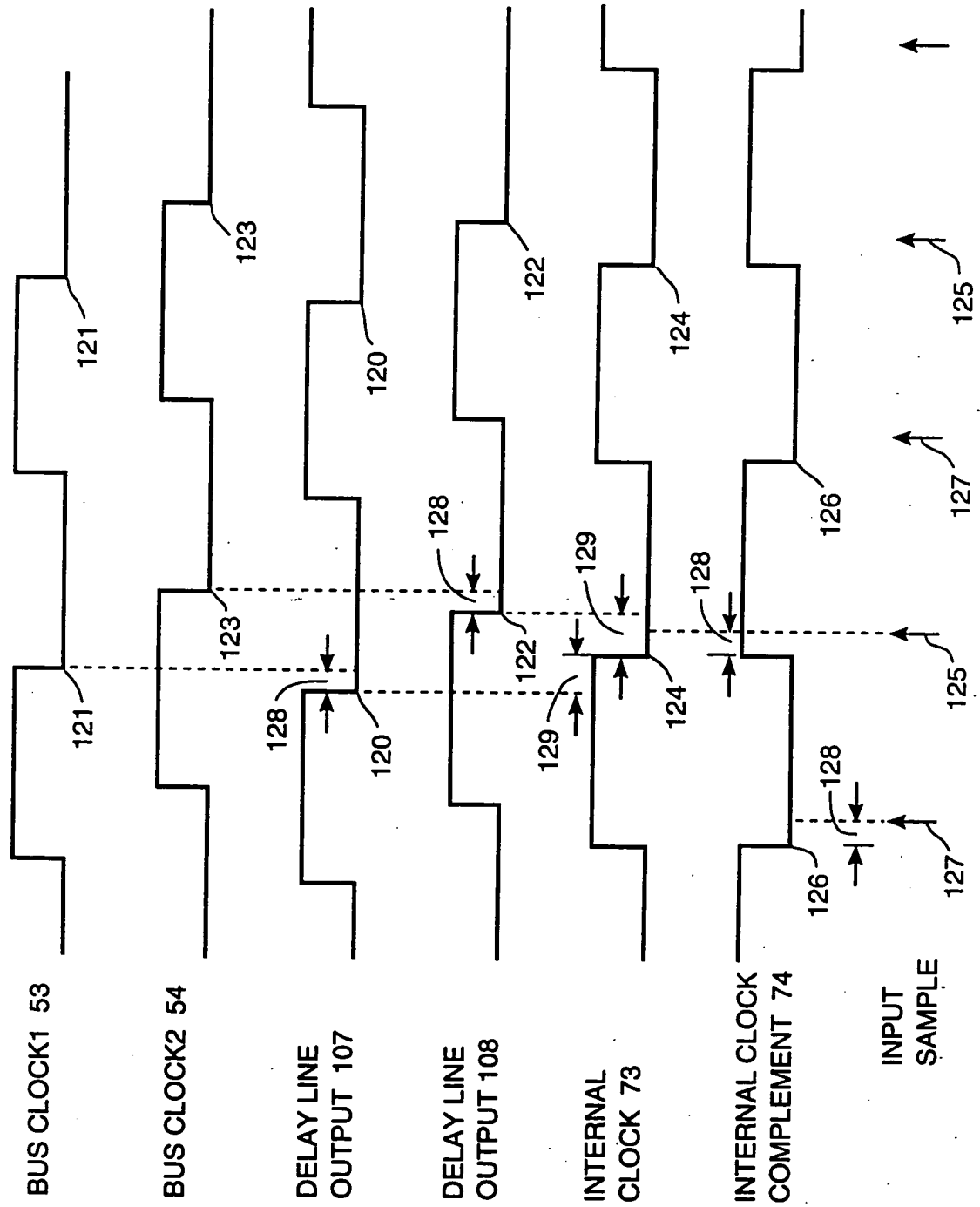


FIG 13



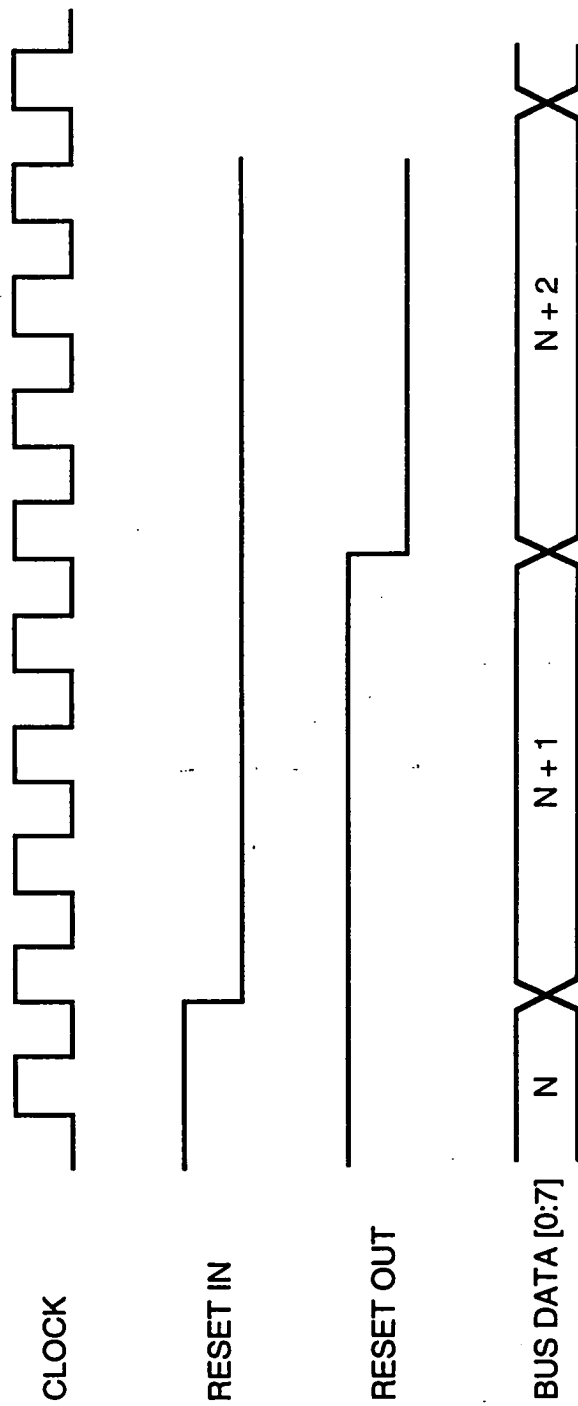


FIG 14

FIG 15

